AMENDMENTS TO THE DRAWINGS

The attached sheet of drawings, which includes Figures 8 and 10-13, replaces the original sheets including Figures 8 and 10-13.

Attachment: Replacement Sheet (Figures 8 and 10-13)

REMARKS

Claims 1-8 are pending in this application. Claim 1 is independent. Claims 1 and 3 are amended. Reconsideration and allowance of the present application are respectfully requested.

Drawings

New drawings have been submitted in response to the Examiner's objection in order to comply with CFR 1.121(d). Applicants respectfully request that the Examiner withdraw the objection.

Rejections under 35 U.S.C. §102 – *JIN et al.*

Claims 1 and 2 stand rejected under 35 U.S.C. §102(b) as being anticipated by "On the Power Dissipation in Dynamic Threshold Silicon-on-Insulator CMOS Inverter," IEEE Transactions on Electron Devices, Vol. 45, No. 8, August 1998 ("Jin"). This rejection is respectfully traversed.

Jin allegedly teaches a silicon-on-insular dynamic threshold voltage MOSFET (SOI DTMOS) in FIG. 3. An Input 1 is said to be connected to stage n-1, which allegedly connects to an inverter containing a p-channel transistor and an n-channel transistor. An output 0 is allegedly connected to stage n, and FIG. 3 is said to further include a source Vdd and a source GND. (Jin, pages 1717-1718).

The Examiner alleges FIG. 3 Jin anticipates claim 1. However, the amended claim 1 includes "a current source connected with the p-type base terminal of the n-channel MOS transistor" and "a current source connected with the n-type base terminal of the p-channel MOS transistor," which the Examiner acknowledges Jin does not teach or suggest (Office Action, page 4). Therefore, because Jin does not teach or suggest all limitations of claim 1, Jin cannot anticipate claim 1 according to M.P.E.P. §2131.

Therefore, Applicants respectfully request the rejection under 35 U.S.C. §102 be withdrawn from claim 1 and claim 2, at least by virtue of its dependency upon claim 1.

Rejections Under 35 U.S.C. § 103 – *JIN in view of YAMAGUCHI*

Claims 3-8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Jin in view of U.S. Patent No. 5,557,231 ("Yamaguchi"). This rejection is respectfully traversed.

Yamaguchi allegedly teaches a bias selecting circuit 32' in FIG. 13. The bias selecting circuit 32' is said to include an NMOS transistor 323 responsive to the control signal CNT for selecting the substrate bias VBB3, and an NMOS transistor 324 responsive to the control signal CNT for selecting the substrate bias VBB4. (Yamaguchi, col. 12, lines 51-59). The bias selecting circuit 32' allegedly also includes NMOS transistors 321 and 322, and the NMOS transistor 321 is said to have its source connected to receive the substrate bias VBB1, its drain connected to a silicon substrate 1 together with the drain of the NMOS transistor 322, and its gate connected to receive the control signal CNT. The NMOS transistor 322 allegedly has its source connected to receive the substrate bias VBB2, and its gate connected to receive the signal CNT. (Yamaguchi, col. 11, lines 17-25; presented with respect to FIG. 8 but incorporated into FIG. 13 in col. 12, lines 58-59).

The Examiner asserts it would be obvious to one of ordinary skill in the art at the time the invention was made "to have used the controlled transistors taught by Yamaguchi in the inverter taught by Jin to reduce current consumption and increase the speed of operation in the inverter circuit (column 4, lines 11-16)." (Office Action, page 5) (*emphasis added*). However, a *prima facie* case of obviousness according to M.P.E.P. §706.02(j) requires that all of the claimed features either taught or suggested by the combination of the references. The Examiner has failed to establish a *prima facie* case of obviousness because Yamaguchi allegedly teaches two current sources connected with two NMOS transistors (321 & 323), not "a current source connected with the p-type base terminal of the **n-channel MOS transistor**" and "a current source connected with the n-type base terminal of the **p-channel MOS transistor**" recited in the amended claim 1. Therefore, the Examiner has failed to establish a *prima facie* case of obviousness and Applicants respectfully request the rejections of claims 3-8 be withdrawn.

Rejections Under 35 U.S.C. § 103 – *JIN in view of YAMAGUCHI & SHIMOMURA et al.*

Claims 5-8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Jin in view of Yamaguchi, and in further view of Japanese Patent Publication No. 10-189957 ("Shimomura"). This rejection is respectfully traversed.

Applicants submit that nothing in Shimomura cures the deficiencies of Jin and Yamaguchi discussed above, and respectfully request that this rejection of claims 5-8 be withdrawn.

CONCLUSION

In view of the above remarks and amendments, Applicants respectfully submit that each of the rejections has been addressed and overcome, placing the present application in condition for allowance. A notice to that effect is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to contact the undersigned.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Donald J. Daley at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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By 

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